Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims

1. (currently amended) Data link layer device for a serial communication bus~~, in particular IEEE1394 bus,~~ comprising an interface to a physical layer unit and an interface to at least one host processor supporting the higher layers of the OSI/ISO data communication reference model, wherein, the data link layer device further comprises means for checking whether a cycle master capable of transmitting a cycle start packet ~~determining minimum start times~~ for isochronous and asynchronous data transmissions over the serial communication bus exists in the network, ~~and if not activating~~ comprising

configuration means that enable the generation of asynchronous transmission requests without waiting for ~~a cycle start packet and~~ an isochronous data transfer and a sub-action gap after occurrence of a local cycle sync event in order to support a no cycle master transfer mode, if the means for checking finds that no cycle master exists in the network.

2. (currently amended) Data link layer device according to claim ~~3~~ 1 wherein the means for checking whether a cycle master exists in the network comprises

a memory storing ~~the~~ self-identification packets from all the nodes in the network, and

evaluating means for checking whether, in one of the self-identification packets, an entry is found that indicate~~d~~s that the corresponding node is a contender for an isochronous resource manager.

3. (currently amended) Data link layer device according to claim ~~3~~1, wherein the means for checking whether a cycle master exists in the network comprises

a first counter for counting clock pulses of a reference clock, the counter generating a cycle synchronization event each time after a predetermined counting interval, and

~~comprising~~ a second counter that is incremented each time that no cycle start packet has been received in succession to a cycle synchronization event, thereby activating said configuration means if the second counter reaches a predetermined value.

4. (currently amended) Data link layer device according to claim ~~3~~1 wherein the means for checking whether a cycle master exists in the network comprises

a memory storing the self-identification packets from all the nodes in the network and

evaluating means for checking whether in one of the self-identification packets an entry is found that indicate~~d~~s that the corresponding node is a contender for an isochronous resource manager.

5. (currently amended) Data link layer device according to claim ~~3~~1, wherein the means for checking whether a cycle master exists in the network comprises

a first counter counting clock pulses of a reference clock, the counter generating a cycle synchronization event each time after a predetermined counting interval, and

~~comprising~~ a second counter that is incremented each time that no cycle start packet has been received in succession to a cycle synchronization event, thereby activating said configuration means if the second counter reaches a predetermined value.